BEYOND GEOMETRY CHECKS: CONTEXT-AWARE DESIGN VERIFICATION

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INTRODUCTION

Context-aware physical verification (PV) is a relatively new addition to traditional PV flows, but it has quickly become a critical and essential technology that addresses the increasing complexity of geometrical checks used in both established and emerging integrated circuit (IC) technologies. Traditional verification tools handle either the physical verification of the layout shapes or the electrical verification of the circuits, but not both. Context-aware checks combine the physical layout of a component with its electrical implementation, and analyze that information to evaluate a wide range of design conditions, from advanced design rule compliance to circuit and reliability verification to design optimization and finishing.

Context-aware PV checks began as an extension to basic design rule checking (DRC) spacing checks, but quickly evolved to address the demanding process and reliability requirements of today's designs. Figure 1 illustrates how context-aware checks can go beyond simple polygon width, spacing, and run length requirements to consider the nets enclosing those polygons and their associated voltage domains when determining DRC compliance [1-4]. For example, in voltage-aware DRC (VA-DRC), the electrical aspects of spacing checks (using either the absolute or delta voltages of the nets) is included when determining spacing compliance. This contributes to improved net reliability without over-constraining the spacing and overall design area.

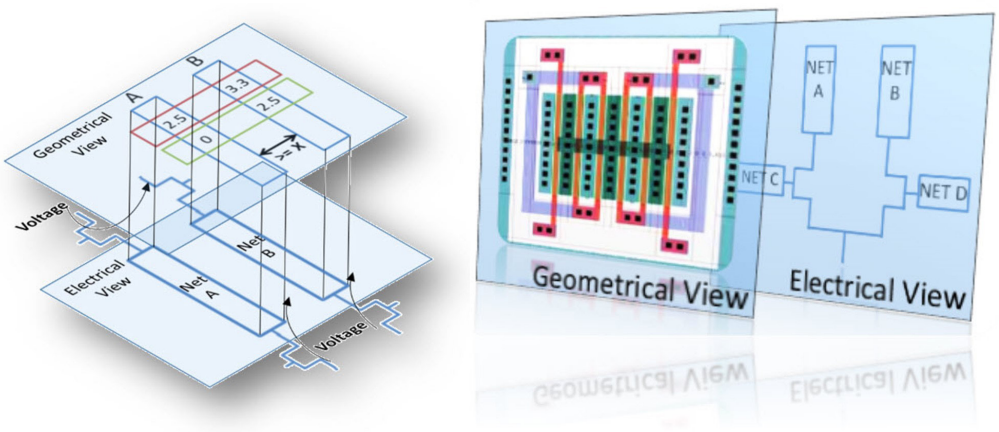

Figure 1: Context-aware checks combine geometrical and electrical aspects to determine design rule compliance.

Beyond DRC, context-aware verification adds a new dimension to other verification flows. The challenges that can be solved with context-aware verification flows increase as technology nodes advance, layouts become smaller and more tightly packed, and design/application requirements get more complex in terms of the number of power domains, nets, and patterns, and their complexity and variability. For example, rather than defining critical layout patterns based only on optical proximity correction (OPC) hotspots or silicon failures, context-aware flows extend the pattern library with electrically-driven patterns, such as differential pairs, current mirrors, silicon photonics structures, and others.

However, invoking context-aware checks without automated support requires the designer to analyze and select the electrical components, cross-reference them between front/back-ends, and manually add marker layers and layout annotations, which is time-consuming and subject to human error. Given the growth in the type and number of context-aware checks, the manual approach is no longer viable.

AUTOMATED CONTEXT-AWARE CHECKING

The Calibre® platform, offering traditional and equation-based DRC verification, design for manufacturing (DFM) design optimization, pattern matching, layout vs. schematic (LVS) verification, and reliability verification, is an established, proven set of tools that can perform topological checks on the schematic side and cross-reference the results to the layout side, enabling fast, accurate, automated context-aware physical verification. Leveraging the logic-driven layout framework in the Calibre PERC™ reliability platform [5,6] to automatically analyze design infrastructure (such as device/net information or device positioning) and combine that information with automated layout annotation, the Calibre platform enables designers to easily and efficiently incorporate these contextual checks into their verification flows (Figure 2). The Calibre PERC topological checks are versatile programmable checks that allow the user to select sections of the netlist by name, structure, or even pre-defined topological patterns that are spread across the design cells and hierarchies. Calibre PERC front-end checking also includes automated static voltage propagation that identifies the voltage domains based on the real circuits [7].

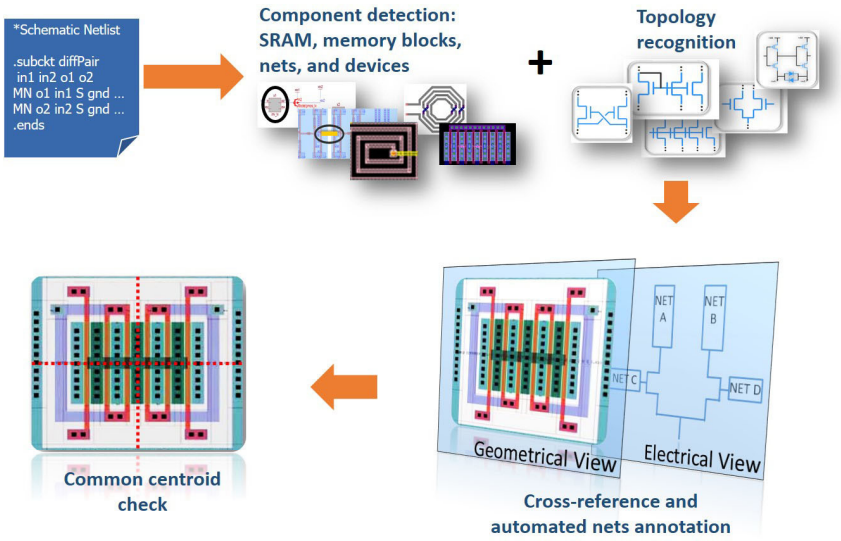

Figure 2: The Calibre PERC platform provides the infrastructure and automation required for context-aware checking, such as common centroid assessment.

Not only does the Calibre platform provide automated contextual checking, but the actionable results it returns also provide designers with the information they need to precisely and accurately adjust the layout. The Calibre platform leverages its integration with the LVS cross-reference database, equation-based DRC, and different DFM property types to enhance error results by tagging them with electrical information (such as source net name, voltage domains, hotspot ID, etc.). For example, in DRC, spacing violations are no longer between two polygons, but between two nets annotated by their source information and topological groups. In failure analysis, hotspot/defect results can be associated with their interacting nets, devices, and even their voltage domains. This data provides the end-user with actionable feedback that improves the quality, accuracy, and turnaround time of debugging.

Similar to the evolution in the design phase that required new layout-aware design techniques, where both the front-end (schematic) and back-end (layout) are implemented simultaneously to account for layout proximity effects and stress parameters, automating context-aware checks means they are no longer limited to geometrical checking, but are now integrated with every stage in the design and verification cycle. For example, designers can combine Calibre PERC electrical pattern matching with Calibre Pattern Matching functionality to detect a differential pair in the netlist (across different hierarchies), and cross-reference the pair to the layout to

perform advanced checks (e.g., layout variants of the same schematic topology, symmetry, matching, common centroid, etc.). Figure 3 displays just a few of the uses for automated context-aware across the design cycle, starting with checking implementation (automated topology recognition with symmetry checking and debugging layout variants of the same schematic topology). These symmetry checks are isomorphic, meaning they can work on single component electrical matching, or analyze the X/Y and common centroid symmetry of a group of components. Other uses include advanced physical verification (VA-DRC), circuit and reliability verification (e.g., context-aware latch-up) [8], DFM and design finishing (e.g., net-aware annotation and filling, via strapping fill, orientation-aware fill) [9,10], and yield/failure analysis.

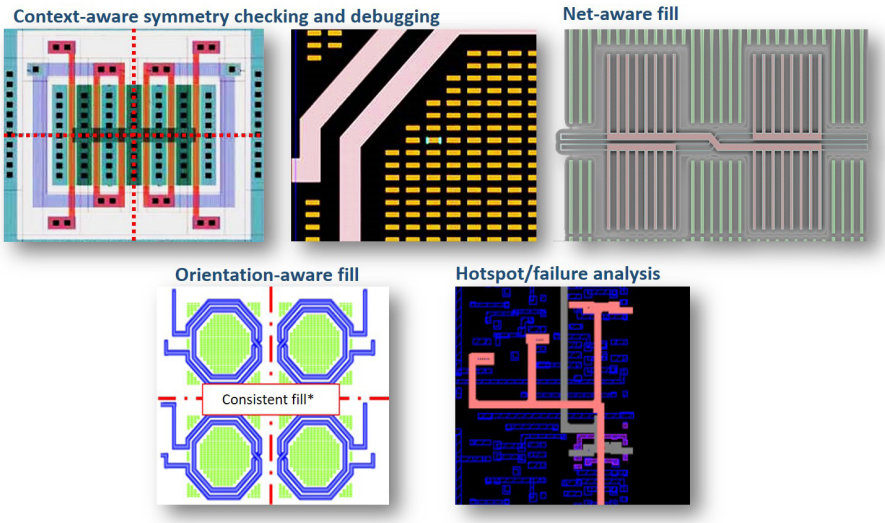

Figure 3: The Calibre PERC platform enables designers to easily add context-aware checking and design enhancement to every step of the design, verification, and test cycle.

CONCLUSION

Context-aware PV flows have been developed to solve demanding design and manufacturing challenges in both established and emerging nodes. However, implementing context-aware checking manually is both laborious and error-prone. The Calibre platform, with the proven ability of the Calibre PERC reliability platform to perform automated context-aware verification, is being used extensively in this and other domains. With capabilities such as automated voltage propagation, topological pattern recognition, and integration of both physical and electrical information within its logic-driven layout framework, this platform can be leveraged for fast, accurate context-aware checking in all phases of design verification.

Utilizing flows where the Calibre PERC infrastructure leverages existing DRC, pattern matching, and LVS capabilities with integrations to other electronic design automation (EDA) tools, designers can easily perform automated context-aware checks from their traditional physical verification and fill flows. Designers can now leverage the actionable net/device debug information provided in error results to more quickly and easily adjust layouts based on both the electrical and geometrical aspects in a design, improving both debugging efficiency and verification precision. As products with greater complexity are developed and consumers demand increasing performance and reliability, the use of automated context-aware checking has become an essential best practice for providing reliable and timely products to the market.

REFERENCES

[1] Dina Medhat, "Automated Solution for Voltage-Aware DRC," EE Times. December 23, 2015. https://www.eetimes.com/author.asp?section_id=36&doc_id=1328540

[2] Mentor, a Siemens Business. "Running Voltage-Aware DRC Checks using Calibre PERC." https://www.mentor.com/products/fv/multimedia/overview/running-voltage-aware-drc-checks-using-calibre-perc-806f401d-b106-4dee-9afe-615e54afca16

[3] Matthew Hogan, "Improve Reliability with Accurate Voltage-Aware DRC," Mentor, a Siemens Business. September, 2013. http://go.mentor.com/4gri5

[4] Sherif Hany, "Calibre PERC advanced voltage-aware DRC delivers exacting accuracy for today's complex designs," Mentor, a Siemens Business. December, 2018. http://go.mentor.com/54eVN

[5] Kollu, K., Jackson, T., Kharas, F., Adke, A., "Unifying Design Data During Verification: Implementing Logic-Driven Layout Analysis and Debug," 2012 IEEE International Conference on IC Design & Technology (ICICDT), pp.1,5, May 30 2012-June 1 2012. http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6232874&isnumber=6232832

[6] P. Gibson, Ziyang Lu, F. Pikus and S. Srinivasan, "A framework for logic-aware layout analysis," 2010 11th International Symposium on Quality Electronic Design (ISQED), San Jose, CA, 2010, pp. 171-175. http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5450415

[7] M. Hogan, S. Srinivasan, D. Medhat, Z. Lu and M. Hofmann, "Using static voltage analysis and voltage-aware DRC to identify EOS and oxide breakdown reliability issues," 2013 35th Electrical Overstress/Electrostatic Discharge Symposium, Las Vegas, NV, 2013, pp. 1-6. http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6635948&isnumber=6635896

[8] Matthew Hogan, "Automated and Context-Aware Latch-Up Checking with the Calibre PERC Reliability Platform," Mentor, a Siemens Business. June, 2017. http://go.mentor.com/4T5a9

[9] D. Kim, E. de la Garza, M. Ibrahim, S. Hany Mousa, M. Hogan, "Improving Analog and RF Fill Generation using Calibre PERC, YieldEnhancer and Pattern Matching," 2017 Design Automation Conference (DAC). June 2017, Austin, TX. http://soiconsortium.eu/wp-content/uploads/2018/10/2017_0616_GF-Fill-Flows-with-Calibre-DAC2017_v1.4-FINAL.pdf

[10] Sherif Hany, "Combine Pattern Matching with DFM to Optimize Layouts," Electronic Design. April 26, 2018. https://www.electronicdesign.com/embedded-revolution/combine-pattern-matching-dfm-optimize-layouts

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